复习题 一

一 判断题

1 A product expression for all sum terms of a logic function must be 0 (T)

2 The output of an exclusive gate with inputs A,B is a 1 (HIGH) when A = 0 and B = 0(F)

3 The output expression for an AND-OR circuit having one AND gate with input A,B,C and D and one AND gate with input E and F is ABCDEF (F)

4 A full-adder is characterized by two inputs and one outputs (F)

5 If an S-R latch has a 0 on the S input and a 1 on the R input and then the S input goes to 0,the latch will be reset (F)

二 单选题

1 To expand a 4-bit parallel adder to an 8-bit parallel adder, you must(D)

A use three 4-bit adders with no interconnections

B use four 4-bit adders and connect the sum outputs of one to the bit inputs of the other

C use two 4-bit adders with no interconnections

D use two 4-bits adders with the carry output of the one connected to the carry input of the other

2 A J-K flip-flop with J = 1 and K = 1 has a 10KHz clock input The Q output is (F)

A constantly LOW

B constantly HIGH

C a 15 KHz square wave

F a 5 KHz square wave

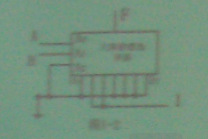
3 8-input data selector multiplexer show in Figure 1-2 the logic function F = (A)

A 非A\*B+A\*非B

B 非A\*非B+A

C AB+B

D AB



4 According to Figure 1- 3 ,the logic expression F = ()

A 非(AB)+BC

B AB+BC

C非(AB)+非(B+C)

D 非(A+B)

5 The relationship of logic function F = A 异或 B and G = A 同或 B is (A).

A F = 非 G

B F = G

C F’ = G

D G 异或 1

6 If a 1-of 16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output.what are the inputs? (C)

A A3A2A1A0 = 1011

B A3A2A1A0 = 1010

C A3A2A1A0 = 1100

D A3A2A1A0 = 0101

7 A 4-bit binary up/down counter is in the binary state of zero .The next state in the DOWN mode is (B)

A 0011

B 1111

C 1001

D 1100

8 the group of bits 10110101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100 After two clock pulses the register contains(C)

A 01011111

B 10110111

C 01111001

D 0110111(少了一位没有拍到)

9 A 4-bit binary up counter counts from 0000, after 1000(dec) clock pulses,the state of counter is (A)

A 1000

B 0101

C 0110

D 1001

10 The AND operation can be produced with (AD)

A Two NAND gates

B Three OR gates

C One NAND gate

D three NOR gates

三 简答题

1 Convert the following decimal numbers to 6-bit two’ binary numbers s complement and add them and give the decimal result.Indicate whether or not the sum overflows a 6-bit result.

1. 8(dec)+18(dec) 001000 + 010010 = 011010(26)
2. -6(dec)+9(dec) 111010 + 001001 = 000011(3)
3. -7(dec)-181(dec) 111001 + (overflow)

2 Convert the Boolean expression F(A,B,C,D) = AC+BC +ACD into standard SOP form

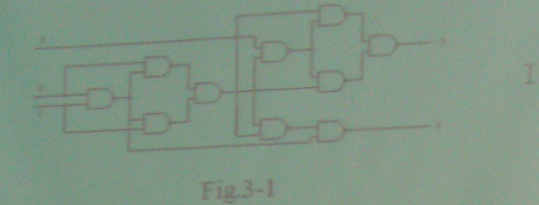
F = ABCD+ABCD+ABCD+ABCD+ABCD+ABCD

3Using Boolean algebra to prove the equation 

Proof:

4 Simplify the Boolean expression with Karnaugh map 

5 Analyze the logic circuit of figure 3-1 write out the logic expression and simplify it

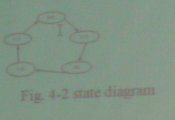


四 综合题

1 分析555定时器

2 一个三位二进制数码由高位至低位分别送至电路的三个输入端,要求三个数码中有两个或两个以上为”1”时, 电路输出为”1”,否则为”0”.试设计并用”与非门”实现这个逻辑电路.

3 Design a counter with the irregular binary count sequence shown in the state diagram of Figure 4-2 Use J-K flip-flop



复习题 二

一 判断题

1 For a given set of input values ,a NOR gate produces the opposite output as a NAND gate(F)

2 if AD=BD is true for logic equation, the A=B is Wrong(T)

3The output of an exclusive-OR gate with inputs A.B is a 0(LOW) when A =1 and B=0(F)

4 On a Karnaugh map , grouping the 0s produce a SOP expression(F)

5 The output expression for an AND-OR circuit having one OR gate with input A,B,C and D and one AND gate with input E and F is ABCD+EF(F)

二 单选题

1 A 4-bit binary up counter counts from 0000, after 100(dec) clock pulses the state of counter is ()

A 1100

B 0001

C 0011

D 0100

2 A J-K flip-flop with J = 1 and K = 1 has a 10 KHz clock input The Q output is ()

A constantly HIGH

B a 5 KHz square wave

C constantly LOW

D a 10 KHz square wave

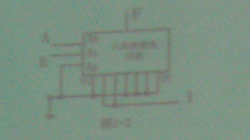
3 A 8-input data selector/multiplexer show in Figure 1-2 the logic function F = ()

A A+B

B 非A\*非B+AB

C AB

D 非A\*B +A\*非B



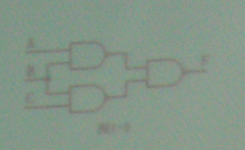
4 According to Figure 1-3 the logic expression F = ()

A 非(AB)\*非(BC)

B 

C 

D AB+BC



5 The relationship of logic function F= A异或 B and G = A 同或 B is ()

A F’ = 非G

B F’ = G

C F = 非G

D F=G 异或1

6 The AND operation can be produced with ()

A Two NAND gates

B Three NAND gates

C One NOR gate

D Three NOR gates

7 A 4-bit binary up/down counter is in the binary state of zero. The next state in the DOWN mode is ()

A 0011

B 0111

C 1110

D 1111

8 The group of bits 10110101 is serially shifted (right-most bit first) into an 8-bit parallel output shift register with an initial state of 11100100 After two clock pulses the register contains ()

A 01111001

B 10110101

C 01011110

D 0101101

9 To expand a 4-bit parallel adder to an 8-bit parallel adder ,you must()

A use two 4-bit adders with the carry output of one connected to the carry input of the other

B use two 4-bit adders and connect the sum outputs of one to the bit inputs of the other

C use eight 4-bit adders with no interconnections

D use four 4-bit adders with no interconnections

10 If a 1-of-16 decoder with active-LOW outputs exhibits a LOW on the decimal 12 output what are the inputs?()

A A3A2A1A0 = 1110

B A3A2A1A0 = 1111

C A3A2A1A0 = 0101

D A3A2A1A0 = 1100

三 简答题

1 Convert the following decimal numbers to 8-bit two’s complement numbers or indicate that the decimal number would overflow the range

1. -76(dec) 10110100
2. -116(dec) 10001100
3. 127(dec) 01111111

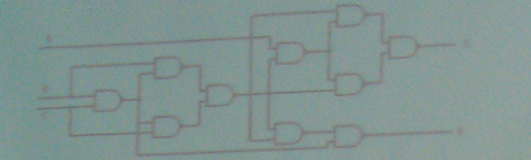
2 Convert the Boolean expression F(A,B,C,D)=AB+CD+AD into standard SOP form

3 Using Boolean algebra to prove the equation

4 Simplify the Boolean expression suing Boolean algebra

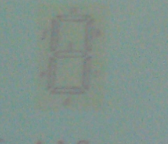
F(A,B,C)= AB+BC+非(BC)+非(AB)

5 Simplify the logic circuit of figure 3-1 and analyze its function

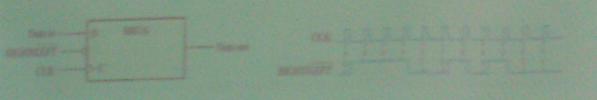


四 综合题

1 Please given the combinational logic circuit of segments 6 for Fig 4-1 7-segment display ,the input is 4-bits binary (Note : the 7-segment display is Common-cathode arrangement)



2 For the 8-bit bidirectional register in Figure 4-2 A HIGN on this input enables a shift to the right and a LOW enalbles a shift to the left Assume that the register is initially storing the decimal number seventy-eight in binary ,with the right –most position being the LSB There is a LOW on the data-input line. Determine the state of the register after each clock pulse for the RIGHT/LEFT control waveform given



3 用与非门设计四变量的多数表决电路,当输入变量ABCD中有3个或3个以上为1 时.输出为1 用红亮表示 输入为其他状态时输出为0 ,灯灭 要求写出真值表 列写表达式 并画出电路图